Product information presented is for internal use within CHIPONE only. Details are subject to change without notice

13-CH LEVEL SHIFTER FOR GOA TFT-LCD PANEL

FEATURES

- **2.6V to 5.5V Input Logic Level Range**
- **-15V to 40V Output Voltage Range**
- **13 Ch Level Shifter Support 8-CH CLK, 2-CH ST, 2-CH LC, VSSG**
- **Protection Functions: UVLO, OTP, OCP**
- **Support 1 CLK IN, 4/6/8 CLK OUT**
- **CLK N/1/2/3 Line Pre-Charge, 1/2/4 Line on**
- **RoHS Compliant and Halogen Free**

GENERAL DESCRIPTION

The iML7278 is a 13 channel high-voltage level-shifter application. The device provides a condense logic that generates 13 outputs signals from the several input signals provided by the Timing Controller (TCON) to high level signals used by the display panel. This outputs are swings from 45V to -20V, high slew rate, and high current driving ability which is fitted for any kind of GOP/GIP/GOA panel. Thermal protection is also designed in this device.

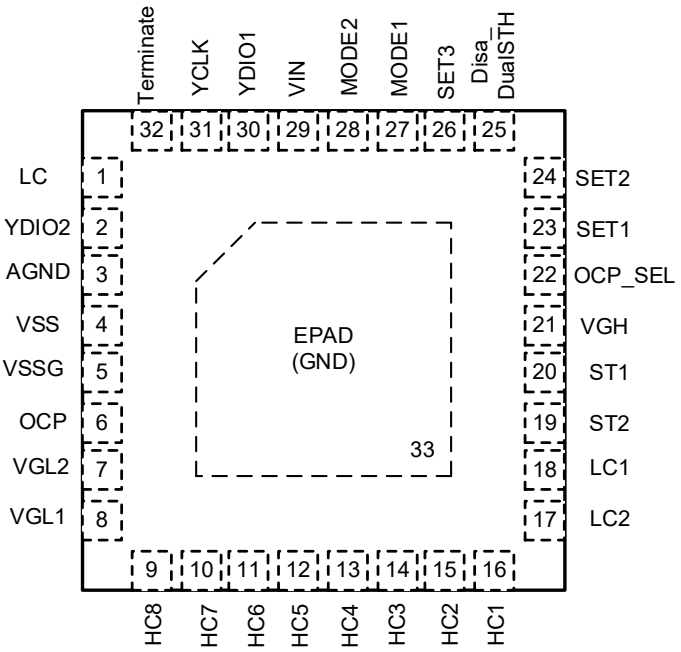
The iML7278 is available in a 32-pin thin QFN package with a maximum thickness of 0.8mm for ultra-thin LCD panels.

The iML7278 is a 13 channel high-voltage maximum thickness of 0.8mm for provides a

APPLICATIONS

GOA TFT-LCD Panel

PIN CONFIGURATION



ORDERING INFORMATION (NEED UPDATED)

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
iML7278	iML7278ID-TR	QFN4x4L_32	Tape and Reel	–40 °C to +85 °C	i7278 XXXXXXX	i7278: Part Name XXXXXXX: Tracking Number.

Note: All CHIPONE products are lead free and halogen free.

TYPICAL APPLICATION

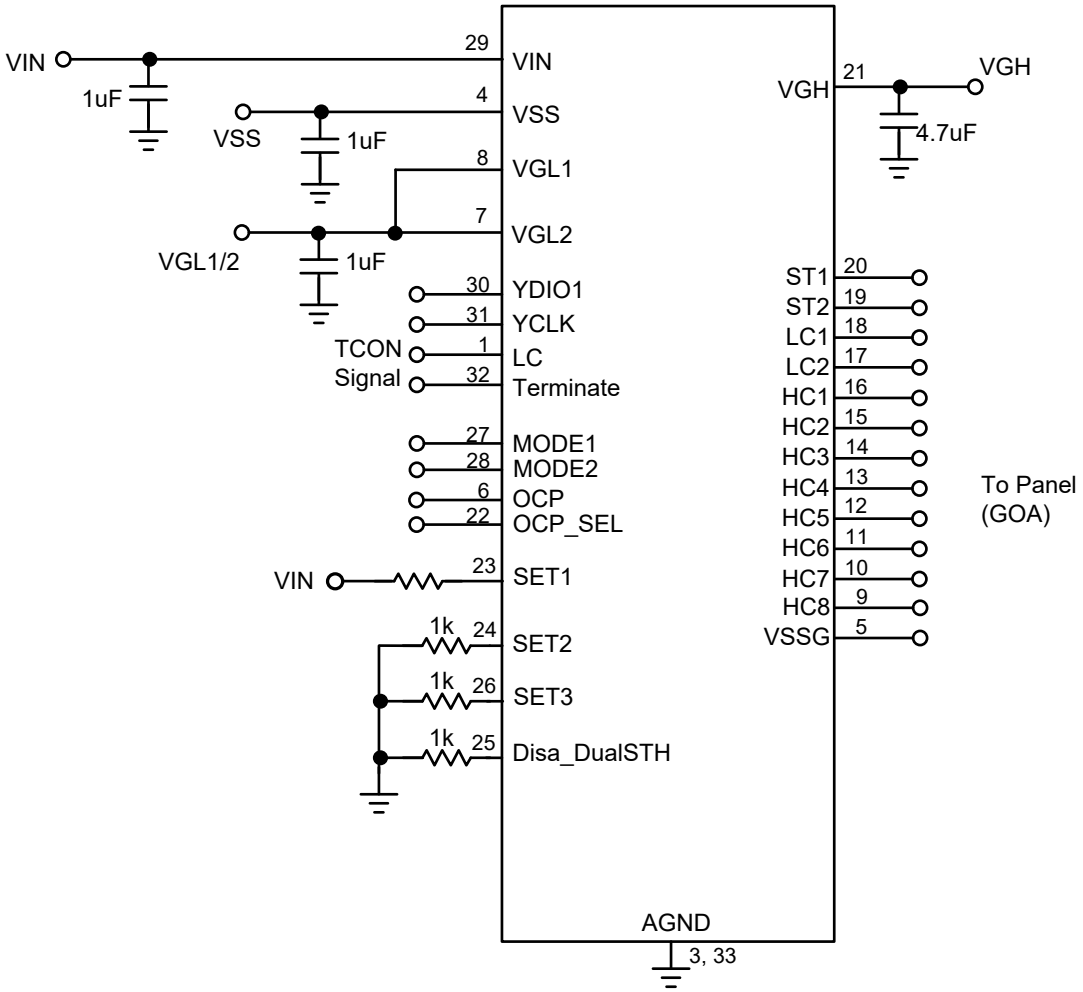


Figure 1.1 The iML7278 Application Circuit

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Input Voltage: VDD(continuous)	V_{IN}	–0.3 to +7	V
Ground Voltage	V_{GND}	–0.3 to +0.3	V
YDIO1, YDIO2, YCLK, MODE1, MODE2, LC, DisaDual_STH, OCP, OCP_SEL, SET1, SET2, SET3, Terminate to GND	V_L	–0.3 to +7	V
VGH to GND	V_{H1}	–0.3 to +45	V
VGL1, VGL2, VSS to GND	V_{H2}	–20 to +0.3	V
(VGH1 or VGH2) – (VGL or LVGL)	V_{H3}	–0.3 to +65	V
ST1, ST2 to GND	V_{H4}	(VGL + 0.3V) to (VGH - 0.3V)	V
HC1~HC8 to GND	V_{H5}	(VGL + 0.3V) to (VGH - 0.3V)	V
LC1, LC2 to GND	V_{H6}	(VGL + 0.3V) to (VGH - 0.3V)	V
VSSG to GND	V_{H7}	(VGL + 0.3V) to (VGH - 0.3V)	V
Power Dissipation, @ T_A = +25°C , T_J = +125°C	P_d	TBD	W
Package Thermal Resistance (Note 2)	θ_{JA}	TBD	°C /W
Package Thermal Resistance (Note 2)	θ_{JC}	TBD	°C /W
Lead Temperature (Soldering, 10sec..)		260	°C
Junction Temperature		150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
ESD Machine Model	MM	400	V
ESD Susceptibility Human Body Model (Note 3) (ST1/2, LC1/2, VSSG, HC1 to HC8 to GND)	HBM	8k	V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Ambient Temperature Range (Note 4)		–40 to +85	°C
Junction Temperature Range (Note 4)		–40 to +125	°C

Notes:

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2. θJA is measured under natural convection (still air) at TA= 25°C with the component mounted on a high effective thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θJC is measured at the exposed pad of the package.

3. Devices are ESD sensitive. Handing precaution is recommended.

4. The device is not guaranteed to function outside its operating conditions.

ELECTRICAL CHARACTERISTICS

DVDD=3.3V, VGH=30V, VGL1=VGL2=-10V, GND=0V, TA=+25°C unless otherwise specified

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Operating Power						
Vin Supply Voltage	VIN		2.6	--	5.5	V
VDD Quiescent Current	IQ-VDD		--	1.4	--	mA
VGH Quiescent Current	IQ-VGH		--	0.3	--	mA
VGL1 Quiescent Current	IQ-VGL1		--	0.3	--	mA
VGL2 Quiescent Current	IQ-VGL2		--	0.1	--	uA
VSS Quiescent Current	IQ-VSS		--	50	--	uA
Protections						
DVDD Under-Voltage Lockout Threshold	$V_{UVLO-VDD}$	VDD rising,	1.9	2.0	2.1	V
		VDD falling	1.7	1.8	1.9	V
		Hysteresis	0.2	0.22		V
VGH1/2 Under-Voltage Lockout Threshold	V_{UVLOGH}	VGH1 rising	6.2		6.9	V
		VGH1 falling	6.0		6.7	V
		Hysteresis	0.2	0.22		
POR Under-Voltage Lockout Threshold	$V_{UVLOPOR}$	POR falling	--	3.5	--	V
Thermal Shutdown	T_{SD}	Junction temperature rising		160		°C
Internal Pull-Down Resistor		Terminate/SET2	300	400	500	kΩ
Internal Pull up/down		SET1	300	400	500	kΩ
Level Shifter						
VGH to GND	VGH		7	--	40	V
VGL1 Operating Voltage Range	VGL1		-15	--	0	V
VGL2 Operating Voltage Range	VGL2	(Note 5)	-15	--	0	V
VSS Operating Voltage Range	VSS	(Note 5)	-15	--	0	V
VGH-VGL1/VGL2/VSS	V_{HL}		--	--	55	V
YCLK, TERMINATE, YDIO1/2, SET2/3, DisaDual_STH, MODE2, LC	VIH	VDD = 2.6V to 5.5V	1.5	--	--	V
	VIL	VDD = 2.6V to 5.5V	--	--	0.8	V
SET1 Input Setting	High	VDD = 2.6V to 5.5V	3		3.6	V

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
	Floating	VDD = 2.6V to 5.5V	1.4		1.9	V
	Low	VDD = 2.6V to 5.5V	0		0.6	V
OCP_SEL Input Setting	High	VDD = 2.6V to 5.5V	3		3.6	V
	Floating	VDD = 2.6V to 5.5V	1.4		1.9	V
	Low	VDD = 2.6V to 5.5V	0		0.6	V
MODE1 Input Setting	Extra-High	VDD = 2.6V to 5.5V	3.3		4	V
	High	VDD = 2.6V to 5.5V	1.7		2.3	V
	Middle	VDD = 2.6V to 5.5V	1		1.3	V
	Low	VDD = 2.6V to 5.5V	0		0.6	V
YCLK, TERMINATE, YDIO1/2, LC Signal Pulse Width (Note 6)	VIW	VDD = 2.6V to 5.5V	200	--	--	ns
YCLK Input signal Maximum Frequency	Fc		--	--	800	kHz
HC1~HC8, ST1/2, and LC1/2 Positive Output Swing	VCK+	All inputs high, IO = 10mA	VGH -0.5	VGH -0.2	VGH	V
ST1/2, and LC1/2 Negative Output Swing	VCK1-	All inputs low, IO = -10mA	VGL1	VGL1 +0.2	VGL1 +0.5	V
HC1~HC8 Negative Output Swing	VCK2-	All inputs low, IO = -10mA	VGL2	VGL2 +0.2	VGL2 +0.5	V
HC1~HC8, ST1/2, LC1/2, and VSSG High-side Switch-on Resistance	RON_{HS}	IO = 10mA		10		Ω
HC1~HC8, ST1/2, and LC1/2 Low-side Switch-on Resistance	RON_{LS}	IO = -10mA		8		Ω
VSSG Low-side Switch-on Resistance	RON_{LS2}	IO = -10mA		2.7		Ω
HC1~HC8, ST1/2, and LC1/2 Rising Slew Rate (Note 7)	t_{R1}	VGH = 30V, VGL1=VGL2=-10V, RL = 50ohm, CL = 4.7nF, 10% to 90%			700	ns
HC1~HC8, ST1/2, and LC1/2 Falling Slew Rate (Note 7)	t_{F1}	VGH = 30V, VGL1=VGL2=-10V, RL = 50ohm, CL = 4.7nF, 90% to 10%			700	ns
HC1~HC8, ST1/2, and LC1/2 Rising / Falling Edge Delay Time	tRD	VGH = 30V, VGL1=VGL2=-10V, 50% of input to 10% of output	--	150	250	ns
	tFD	VGH = 30V, VGL1=VGL2=-10V, 50% of input to 90% of output	--	150	250	ns
HC1~HC8, STH1/2 High/Low Side Blanking Time	STH/CLK_{bt}			4		us
HC1~HC8 High/Low Side, STH1/2 High Side Detect Time	STH_H/CLK_{dt}			1.5		us

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
STH1/2 Low Side Detect Time	STH_L_{dt}			512		us
LC1/2 High/Low Side Blanking Time	LC_{bt}		--	512	--	us
LC1/2 High/Low Side Detect Time	LC_{dt}		--	512	--	us
VSSG Low Side Detect Time	$VSSG_{dt}$		--	512	--	us
HC1~8, STH1/2, LC1/2 High/Low Side, and VSSG Low Side OCP Triggered Level		OCP_SEL=High		180		mA
		OCP_SEL=Floating		100		mA
		OCP_SEL=Low		60		mA

Notes

5.The sequence of VGL1 must be earlier than (or equal to) VGL2 in application. The voltage of VGL1 must be lower than (or equal to) VGL always. If VGL1-VGL2>0.3V, abnormal IC function behavior maybe happen.
6.The input signal pulse width must be over 200ns.
7. Rising/Falling time measure point is before RC.

PIN DESCRIPTION

PIN #	NAME	I/O	DESCRIPTION
1	LC	I	Level Shifter Input Signal(Low Frequency Clock)
2	YDIO2	I	Level Shifter Input Signal(Start Pulse for GOA Share) Rising/Falling Edge Trigger.
3	AGND	-	Analog Ground for Logic Block.
4	VSS	P	Negative Power Supply for VSSG Output
5	VSSG	O	Discharge Function for Liquid Crystal Capacitor.
6	OCP	I	Disable Control Input of Short Protection Function. The Setting will Trigger & Latch the Phase Selection Function by Each YDIO1 Rising Edge. Level / OCP status High / OCP disabled Flating/Low / OCP enabled
7	VGL2	P	HC1~8 Negative Power Supply.
8	VGL1	P	ST1/2, LC1/2 Negative Power Supply.
9	HC8	O	Level Shifter Output.
10	HC7	O	Level Shifter Output.
11	HC6	O	Level Shifter Output.
12	HC5	O	Level Shifter Output.
13	HC4	O	Level Shifter Output.
14	HC3	O	Level Shifter Output.
15	HC2	O	Level Shifter Output.
16	HC1	O	Level Shifter Output.
17	LC2	O	Level Shifter Output.(Low Frequency Clock 2)
18	LC1	O	Level Shifter Output.(Low Frequency Clock 1)
19	ST2	O	Level Shifter Output.(Start Pulse for GOA Share)
20	ST1	O	Level Shifter Output.(Start Pulse for GOA Charge)
21	VGH	P	ST1/2, LC1/2, HC1~8, VSSG Positive Power Supply.
22	OCP_SEL	I	Setting Pin for OCP Level. High: 180mA Floating: 100mA Low: 60mA

<table>
<tr><td>23</td><td>SET1</td><td>I</td><td>Setting Pin for Phase Selection.
High: 8 Phase
Floating: 4 Phase
Low: 6 Phase
The Setting will Trigger & Latch the Phase Selection Function by Each YDIO1 Rising Edge.</td></tr>
<tr><td>24</td><td>SET2</td><td>I</td><td>Setting Pin for Clocks Interval.
High: Some Time Interval Between HCs.
Low/Floating: No Time Interval Between HCs.
The Setting will Trigger & Latch the Phase Selection Function by Each YDIO1 Rising Edge.</td></tr>
<tr><td>25</td><td>Disa_DualSTH</td><td>I</td><td>Setting Pin for Dual STH Output..
High: ST1 On(Follow YDIO1), ST2 Keeps VGL1.
Low/Floating: ST1 On(Follow YDIO1), ST2 On(Follow YDIO2).
The Setting will Trigger & Latch the Phase Selection Function by Each YDIO1 Rising Edge.</td></tr>
<tr><td>26</td><td>SET3</td><td>I</td><td>Setting Pin for HC Line Mode.
<table>
<tr><th>Pin</th><th></th><th></th><th></th><th></th></tr>
<tr><td>Mode2</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Set3</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>function</td><td>1-line on</td><td>1-line on</td><td>4-line on</td><td>2-line on</td></tr>
</table>
The Setting will Trigger & Latch the Phase Selection Function by Each YDIO1 Rising Edge.</td></tr>
<tr><td>27</td><td>MODE1</td><td>I</td><td>Setting Pin for Pre-Charge Selection.
Extra High: 3-Line Pre-Charge
High: 1-Line Pre-Charge
Middle: No Pre-Charge
Low: 2-Line Pre-Charge
The Setting will Trigger & Latch the Phase Selection Function by Each YDIO1 Rising Edge.</td></tr>
<tr><td>28</td><td>MODE2</td><td>I</td><td>Setting Pin for HC Line Mode.
<table>
<tr><th>Pin</th><th></th><th></th><th></th><th></th></tr>
<tr><td>Mode2</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Set3</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>function</td><td>1-line on</td><td>1-line on</td><td>4-line on</td><td>2-line on</td></tr>
</table>
The Setting will Trigger & Latch the Phase Selection Function by Each YDIO1 Rising Edge.</td></tr>
<tr><td>29</td><td>VIN</td><td>P</td><td>Supply Voltage Input.</td></tr>
<tr><td>30</td><td>YDIO1</td><td>I</td><td>Level Shifter Input Signal(Start Pulse for GOA)
Rising/Falling Edge Trigger.</td></tr>
</table>

31	YCLK	I	Level Shifter Input Signal(Condensed Clock) Rising/Falling Edge Trigger.
32	TERMINATE	I	Level Shifter Input Signal. Pull HC1~8 Low in Blanking Time.
33	EPAD	P	The E-Pad Should Be Connected to GND.

THEORY OF OPERATION

General Description

The iML7278 provides 13-channel Level Shifter designed to drive the GOA panel. This device converts the logic-level signals generated by the Timing Controller (TCON) to high-level signals required by GOA panel.

Power On Sequence

When the VIN exceeds UVLO, the internal signal ENA for condensed GOA logic will be high. The outputs of Level Shifter HC1~8 and VSSG should follow VGL2/VSS level since VIN exceeds UVLO. The outputs of Level Shifter LC1/2, ST1/2 should follow VGL1 level since VIN exceeds UVLO. After exceeds VIN UVLO rising, HC1 to HC8 do not output until receiving the first YDIO1 rising edge. After VIN >_UVLO rising and LC rising edge, LC1 and LC2 will follow LC truth table transient.

LC Truth Table		
LC(from TCON)	0	1
LC1	0	1
LC2	1	0

According to GOA circuit experience, it is recommended that 1. LC1 and LC2 start to work earlier than the 1st YDIO by 28us; 2. Logic signal (YDIO, LC, YCLK) must be sent after VGH power ready.
The recommended power-on sequence is VIN (2.6 to 5.5V) → VGL1 → VGL2 → VSS → VGH or VIN (2.6 to 5.5V) → VG1=VGL2 → VSS → VGH.
The concern of IC design is focus on VGL1/2 and VSS ESD diode. The most negative voltage must be ready before the other negative voltage.

Power Sequence

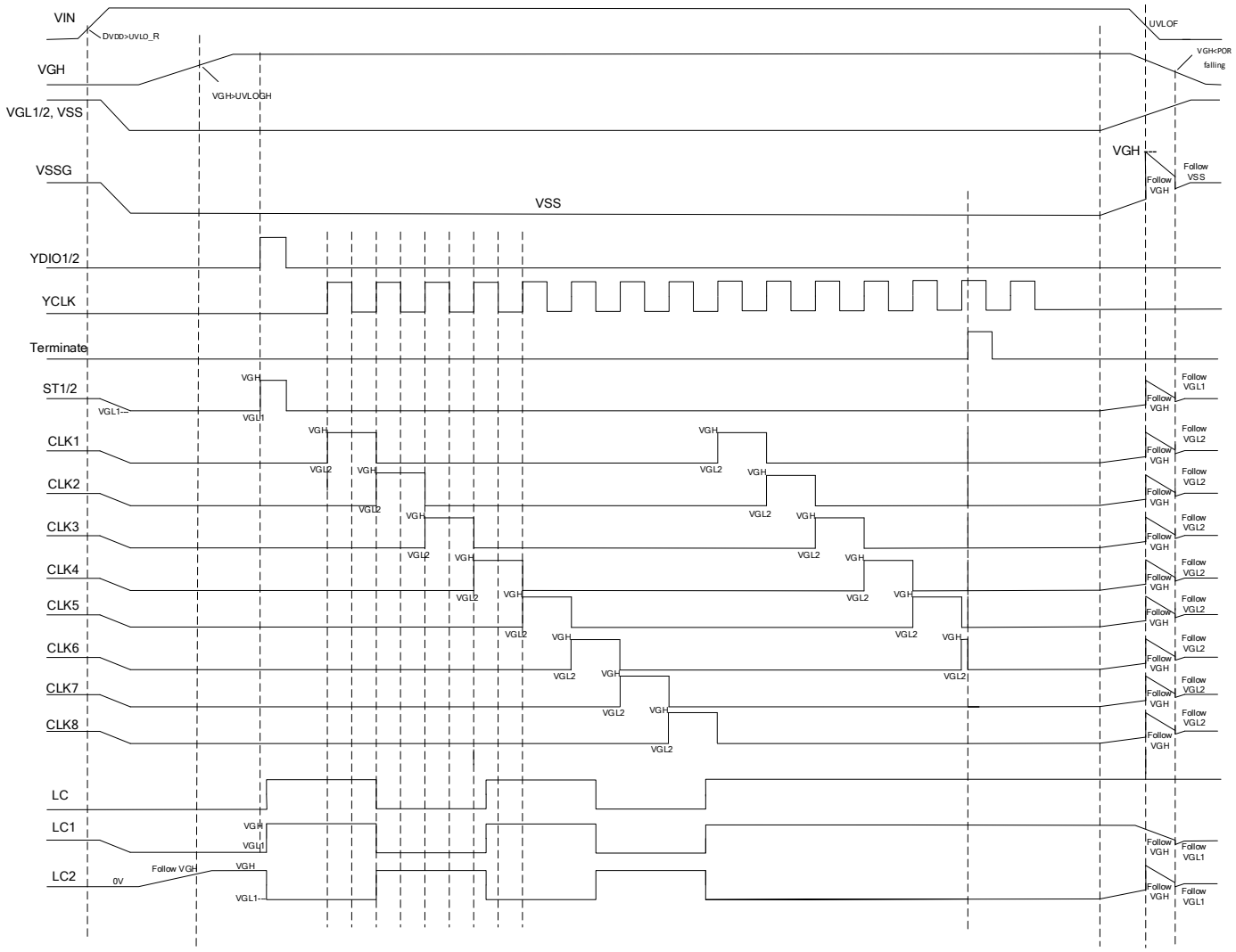


Figure 1. The iML7278 Power Sequence

Table 1 Power On Condition

Case	Analog Power Input			Logic Input				Analog Output				
	VIN	VGH	VGL1/2,VSS	YDIO1	YDIO2	YCLK	LC	ST1	ST2	HC1~8	LC1/2	VSSG
1.1	<UVLO	<UVLO	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	VGL1	VGL1	VGL2	Hi-Z	VSS
1.2	<UVLO	>UVLO	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	VGL1	VGL1	VGL2	LC1=LC LC2=LC_B	VSS
1.3	>UVLO	<UVLO	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	VGL1	VGL1	VGL2	LC1=LC LC2=LC_B	VSS
2.1	>UVLO	>UVLO	Don't Care	w/o	w/o	w/i	w/o	VGL1	VGL1	VGL2	LC1=LC LC2=LC_B	VSS
2.2	>UVLO	>UVLO	Don't Care	w/i	w/o	w/i	w/o	Normal	VGL1	Normal	LC1=LC LC2=LC_B	VSS
2.3	>UVLO	>UVLO	Don't Care	w/o	w/i	w/i	w/i	LVGL	Normal	VGL2	LC1=LC LC2=LC_B	VSS
2.4	>UVLO	>UVLO	Don't Care	w/i	w/o	w/o	w/i	Normal	VGL1	VGL2	LC1=LC LC2=LC_B	VSS
3.1	>UVLO	>UVLO	Don't Care	w/i	w/i	w/i	w/i	Normal	Normal	Normal	LC1=LC LC2=LC_B	VSS

Table 2 Power Off Condition

Case	Analog Power Input			Logic Input				Analog Output				
	VIN	VGH	VGL1/2,VSS	YDIO1 Flag	YDIO2	YCLK	LC	ST1	ST2	HC1~8	LC1/2	VSSG
1.1	<UVLO	>UVLO	Don't Care	Yes	Don't Care	Don't Care	Don't Care	VGH	VGH	VGH	VGH	VGH
1.2	<UVLO	<UVLO	Don't Care	Yes	Don't Care	Don't Care	Don't Care	VGH	VGH	VGH	VGH	VGH
2.1	>UVLO	<UVLO	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	VGL1	VGL1	VGL2	LC1=LC LC2=LC_B	VSS
3.1	<UVLO	>UVLO	Don't Care	No	w/o	w/i	w/o	VGL1	VGL1	VGL2	LC1=LC LC2=LC_B	VSS
3.2	<UVLO	<UVLO	Don't Care	No	w/o	w/i	w/o	VGL1	VGL1	VGL2	LC1=LC LC2=LC_B	VSS

Protection

The iML7278 contains Over-Temperature Protection (OTP), Over-Current Protection (OCP). The following table shows the main behavior of each protection.

Table 3. Over temperature Protection and Over Current Protections

Function / Protection	Output	Recovery
OTP	Hi-Z	VIN<UVLO
OCP	Hi-Z	VIN < UVLO

Over-Temperature Protection (OTP)

An Over-Temperature Protection (OTP) is equipped to prevent C2A038 from overheating due to the excessive power dissipation. The OTP will stop operating while junction temperature exceeds 150°C. Unless the VIN UVLO rising edge comes, the level shifter will keep in Hi-Z state.

Over-Current Protection (OCP)

The iML7278 can detect output pins (ST1/2, HC1~8, LC1/2, VSSG) short to each other short current. If the pin to pin short current over limit, the IC are all outputs (ST1/2, HC1~8, LC1/2, VSSG) will pull high impendence state. After Vin<UVLO falling, IC recovers again.

Timing Diagram

Mode1=Middle(No Precharge), SET1=High(8Phase), SET2=High(Some Time Interval)

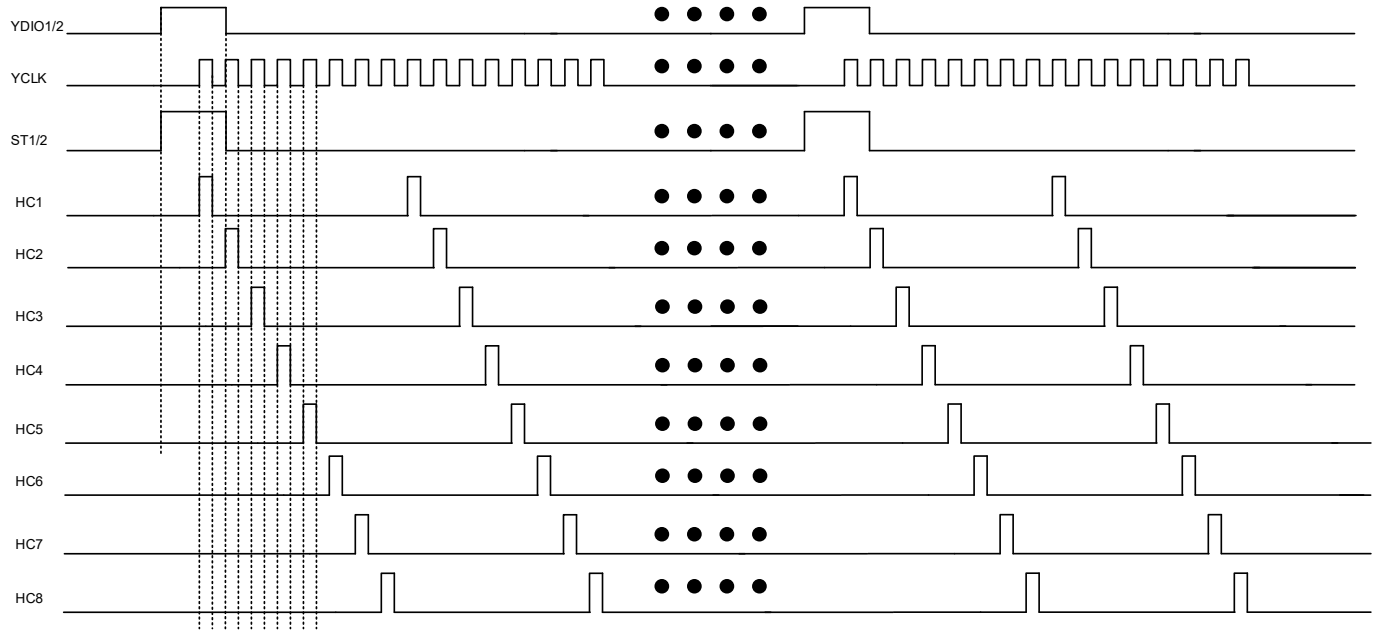


Figure 2. No Pre-charge Timing Diagram

Mode1=High(1 Line Precharge), SET1=High(8Phase), SET2=Low(No Time Interval)

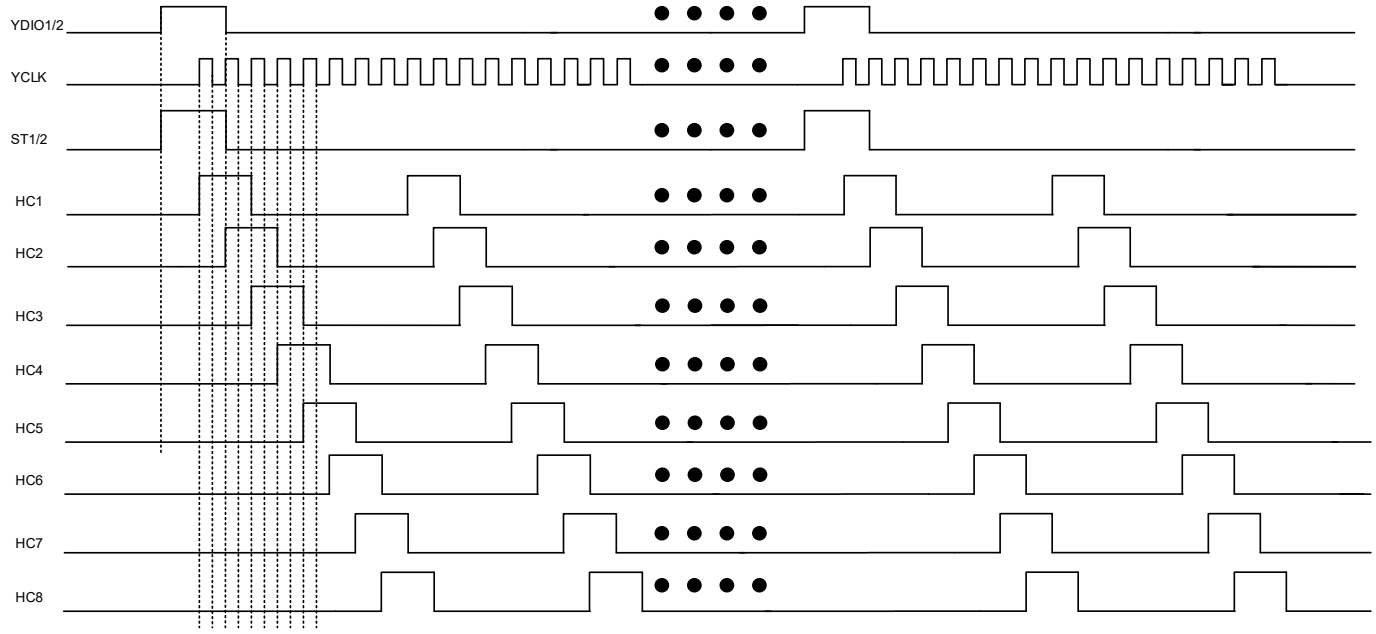


Figure 3. 1 Line Pre-charge Timing Diagram

Mode1=Low(2 Line Precharge), SET1=High(8Phase), SET2=Low(No Time Interval)

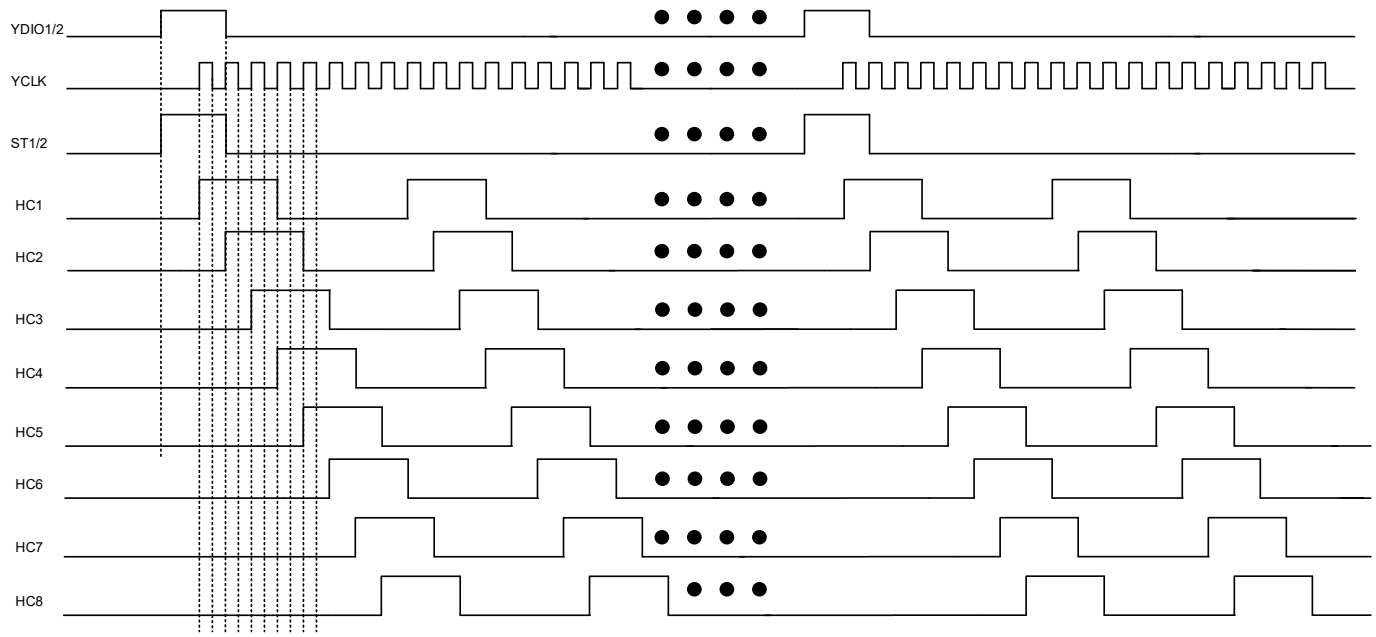


Figure 4. 2 Line Pre-charge Timing Diagram

Mode1=Extra High(3 Line Precharge), SET1=High(8Phase), SET2=Low(No Time Interval)

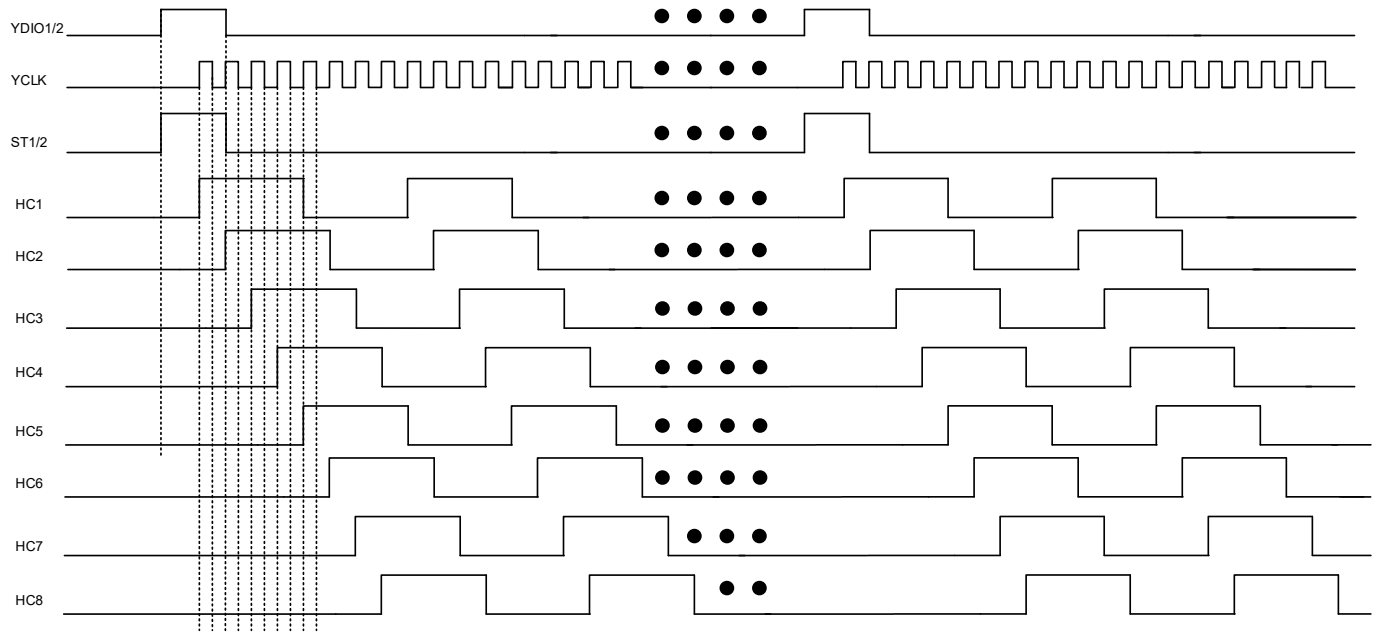


Figure 5. 3 Line Pre-charge Timing Diagram

Mode1=Middle(No Precharge), SET1=High(8Phase), SET2=High(Some Time Interval)

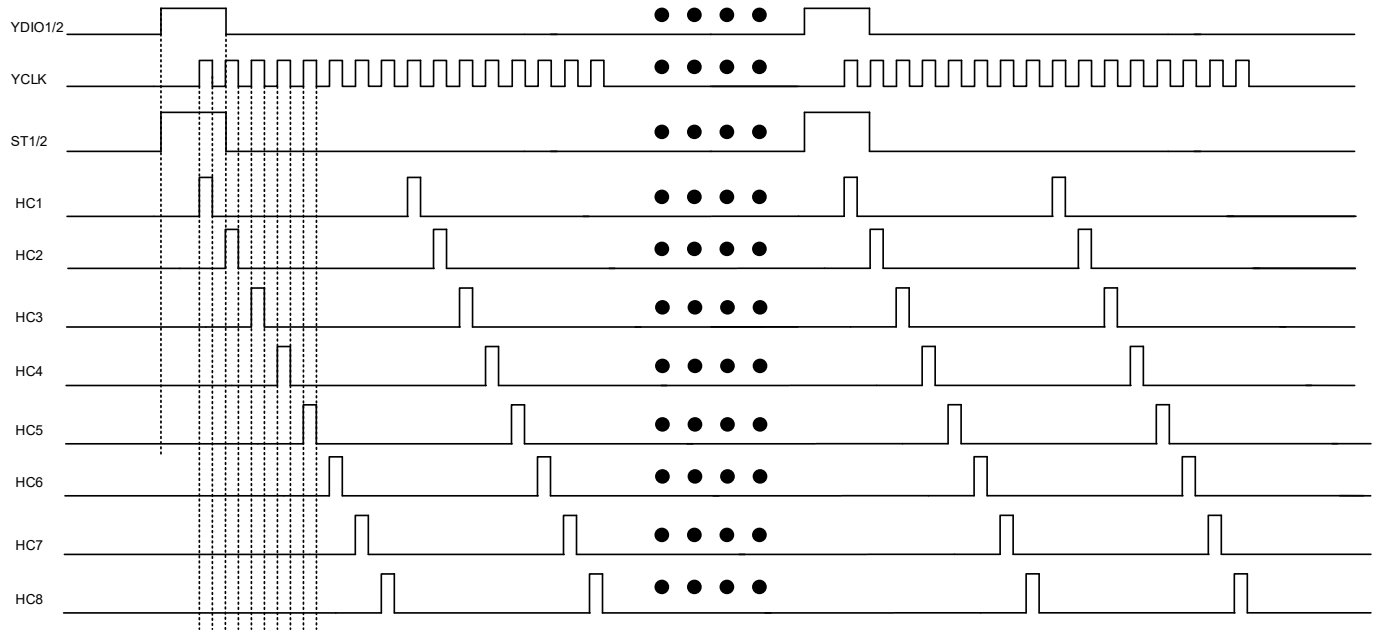


Figure 6. Some Time Interval Timing Diagram

Mode1=Middle(No Precharge), SET1=High(8Phase), SET2=Low(No Time Interval)

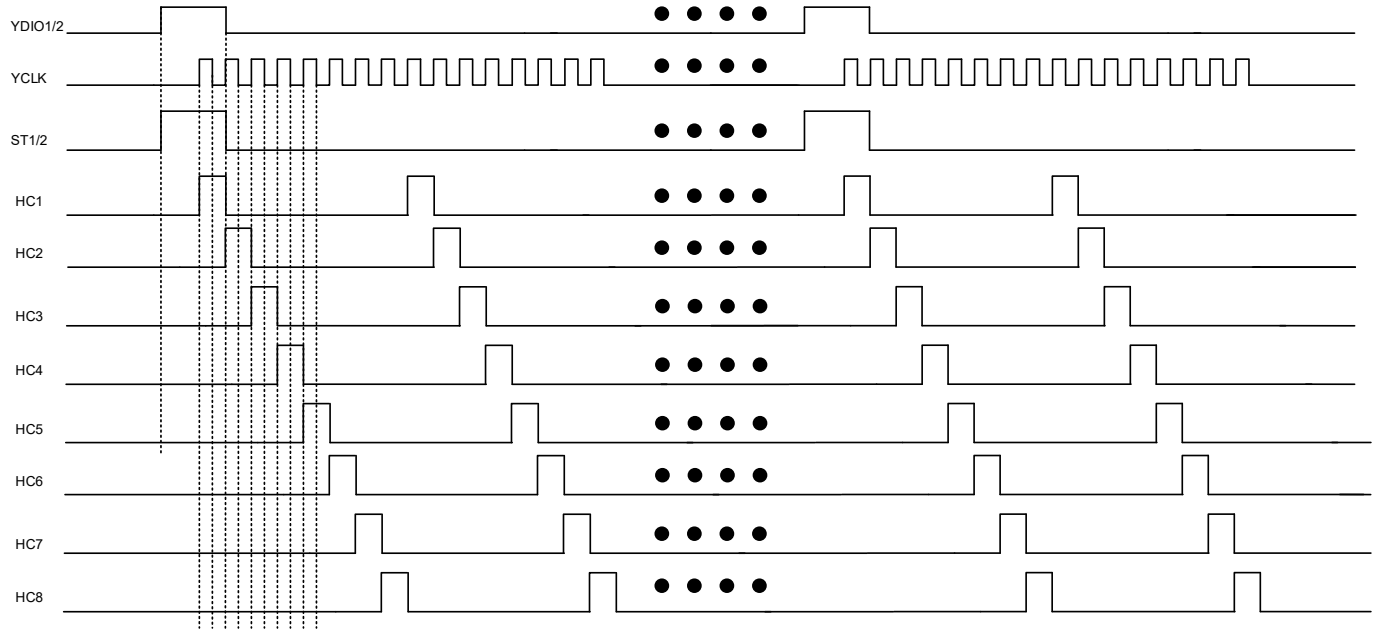


Figure 7. No Time Interval Timing Diagram

Mode1=High(1 Line Precharge), SET1=Low(6Phase), SET2=Low(No Time Interval)

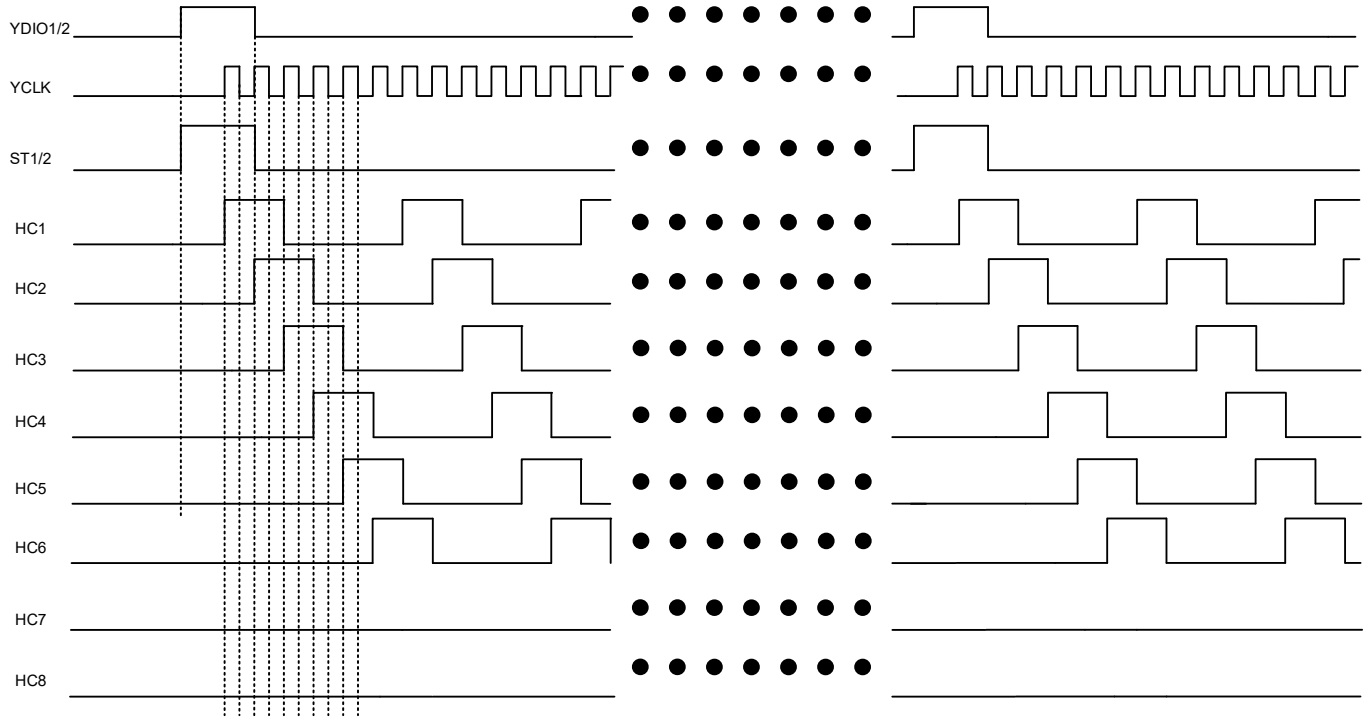


Figure 8. 6 Phase Timing Diagram

Mode1=High(1 Line Precharge), SET1=Floating(4Phase), SET2=Low(No Time Interval)

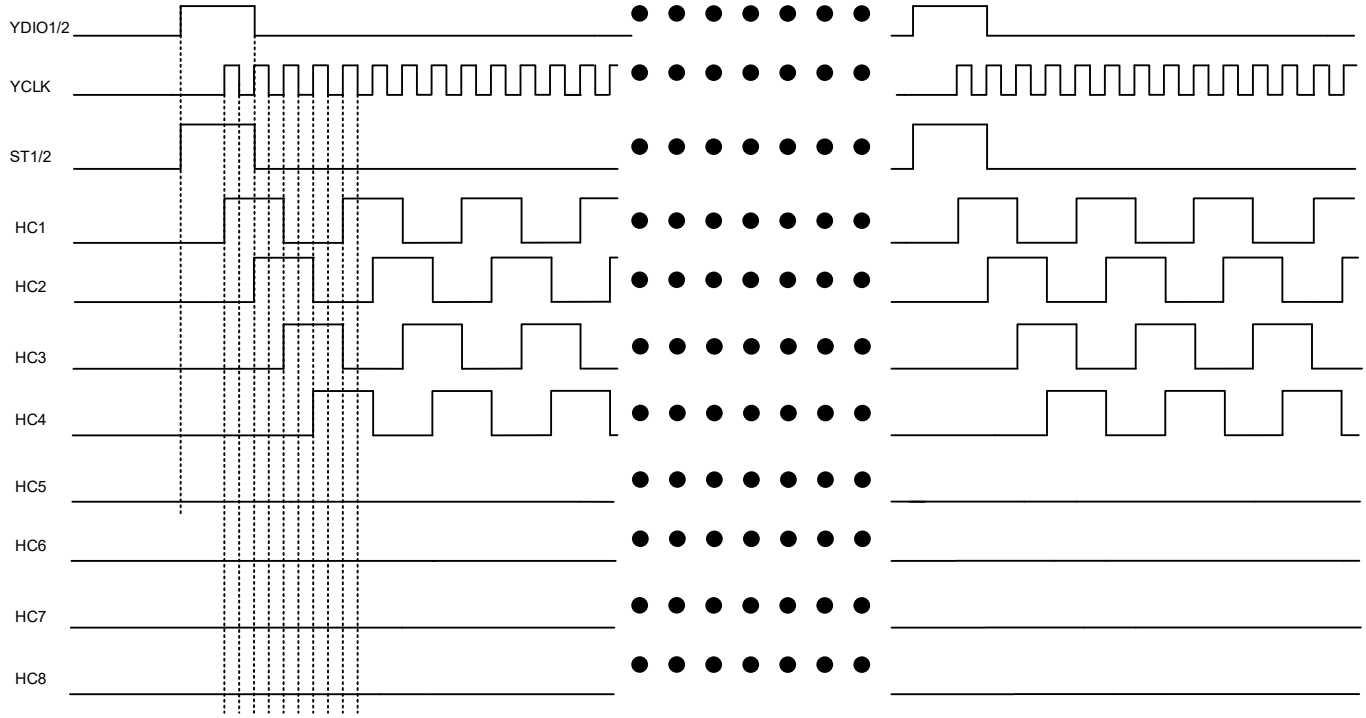


Figure 9. 4 Phase Timing Diagram

Mode1=Low(2 Line Precharge), SET1=High(8Phase), SET2=High(Some Time Interval), 2Line Mode

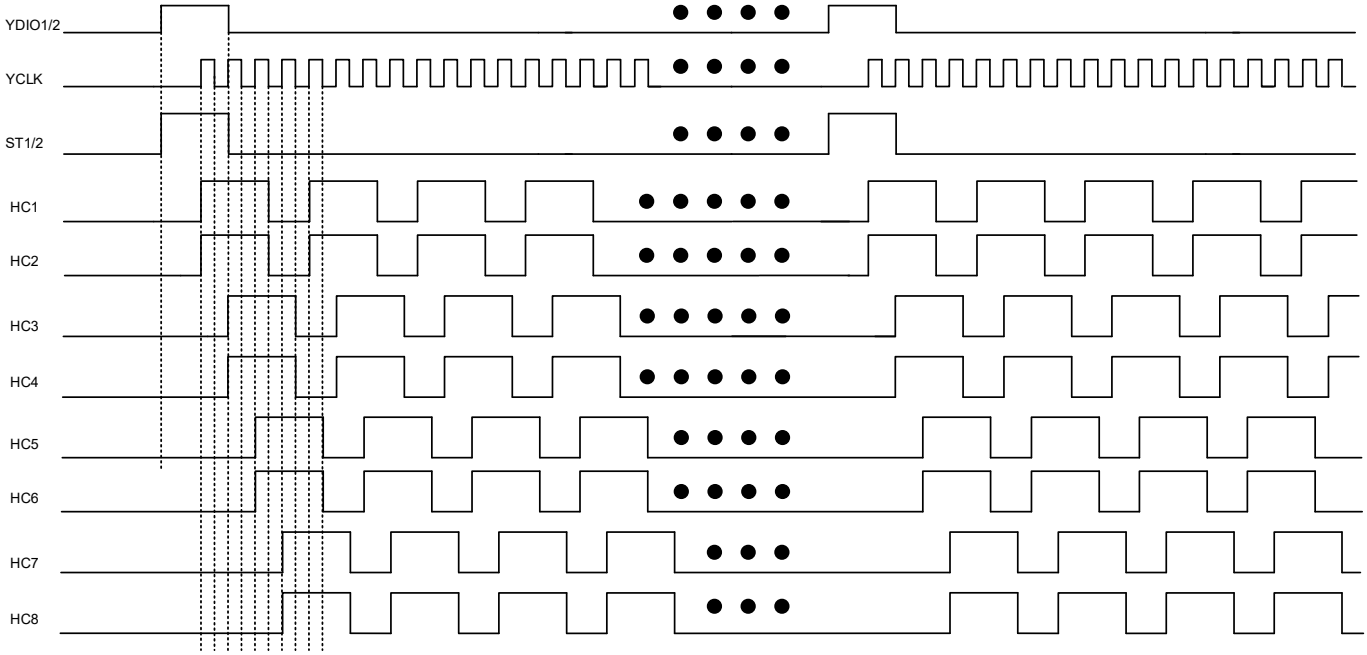


Figure 10. 2Line Mode Timing Diagram

Mode1=Middle(No Precharge), SET1=High(8Phase), SET2=Low(No Time Interval), 4Line Mode

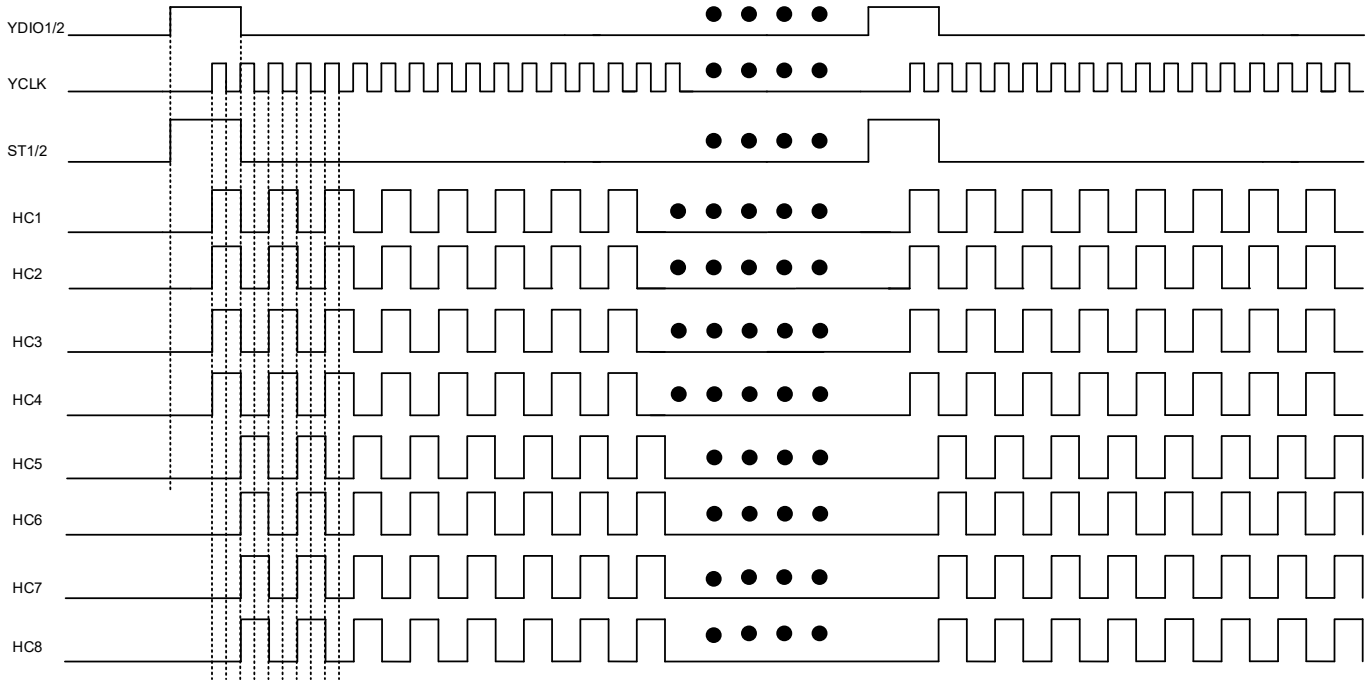
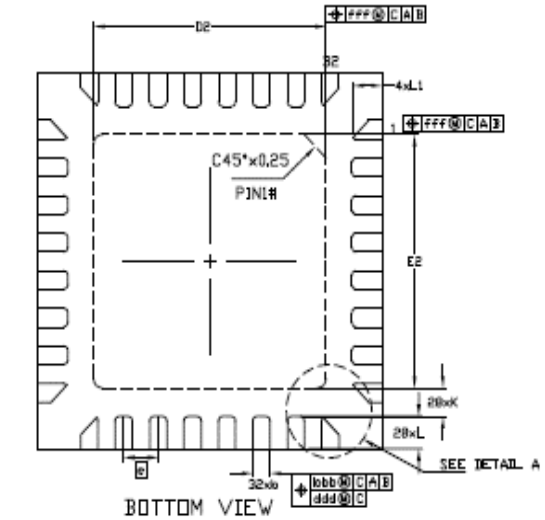
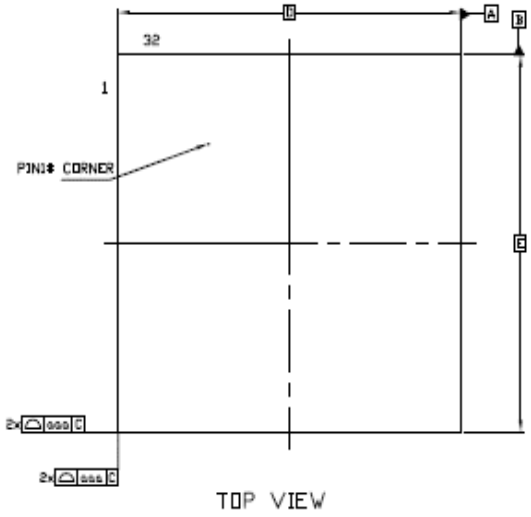
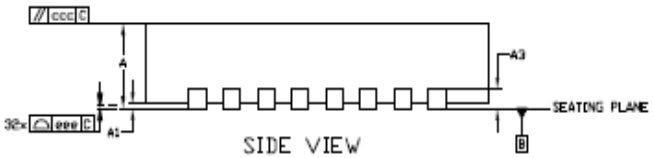


Figure 11. 4Line Mode Timing Diagram

PACKAGE INFORMATION [Drawing is not to scale]







Symbol	Chipone POD		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.60	2.75	2.90
E	3.90	4.00	4.10
E2	2.60	2.75	2.90
e		0.40BSC	
L	0.20	0.30	0.40
L1	0.29	0.34	0.39
K	0.20	-	-
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	